REMARKS

Claims 39-40 are amended. Claims 1-40 are pending and under consideration.

AMENDED CLAIMS

Claim 39 is amended to clarify that the "digital input circuit" is a --data input circuit--.

Claim 40 is amended to correct the antecedent basis in the claim without narrowing the claim.

No new matter is presented and, accordingly, approval and entry of the foregoing amended claims is requested.

PAGES 4-5: ALLOWABLE SUBJECT MATTER

The Examiner has indicated that claims 1-29, 33-38, and 40 are allowed, and Applicants thank the Examiner for such indication of allowability.

ITEM 2: REJECTION OF CLAIMS 30-32 UNDER 35 U.S.C. §102(b) BY HATA (U.S.P. 5,479,455)

Independent claim 30 recites an input signal processing circuit clocked by a first clock signal, inputting one or more first signal(s) including a rising edge of the third clock signal occurring at substantially a same time as a rising edge of the first clock signal and enabling the second latch circuit to enter a responsive state during a non-responsive state of the first latch circuit.

The Examiner contends that Hata describes that a rising edge of the third clock signal occurs at substantially a same time as a rising edge of the first clock signal. (Action at page 2).

Traverse

Anticipation (§102) requires that each and every element as set forth in a claim be described in a single prior art reference i.e. *In re Robertson*, 49 USPQ 2d 1949 (Fed. Cir. 1999).

Rising Edge Of Third Clock Signal At Substantially Same Time As Rising Edge Of First Clock Signal Not Described

Applicant submits that Hata describes that the rising edge of a third clock signal is not at substantially a same time, but rather is substantially delayed relative to the rising edge of a first clock signal. (See, for example, FIG. 15). Hata describes (col. 15, lines 14-42) that a second clock signal and a third clock signal are generated by a circuit shown in FIG. 10 that includes a delay element 18. This delay element 18 causes a rising edge of a third clock signal to be delaying substantially relative to a rising edge of a first clock signal. In addition, a delay introduced by delay element 18 will result in a jitter in a rising edge of a first clock signal. Such a

jitter, introduced by the elements described by Hata, would degrade final signals as recited by claim 30 that are delivered by a second latch to be jitter free.

Input Signal Processing Circuit Performing A Predetermined Processing Operation On a First Signal Not Described.

Claim 30 recites a feature of a first latch circuit inputting an output signal of an input signal processing circuit. In Hata (see, for example FIG. 14), the first signal i.e. the data input signal Din is applied directly to a first latch circuit.

Applicant requests reconsideration and withdrawal of the rejections of independent claim 30 and claims 31 and 32 dependent thereform.

ITEM 39: REJECTION OF CLAIM 39 UNDER 35 U.S.C. §102(b) BY BECHADE ET AL. (5,272,729)

Claim 39 as amended recites a data input circuit receiving a plurality of digital data signals in response to a first clock signal.

Data Signals Not Described

Bechade describes a process independent digital clock signal-timing network for generating a chip clock substantially in phase with, and offset by one cycle from, an input clock signal. (See col. 2, lines 5-20). That is, a plurality of digital signals received by the digital input circuit described in Bechade are simply delayed versions of a first clock signal. Digital data signals are not described in Bechade.

Accordingly, Applicants respectfully request that the rejection of claim 39 be withdrawn.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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